



## Features

- 100Watts Peak Power per Line ( $t_p = 8/20\mu s$ )
- Protects two I/O lines
- Low operating voltage: 5V
- Ultra Low capacitance( $<1.0pF$ ) for high-speed interfaces
- Solid-state technology

## IEC Compatibility (EN61000-4)

- IEC 61000-4-2 (ESD)  $\pm 15kV$  (air),  $\pm 8kV$  (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 4A (8/20 $\mu s$ )



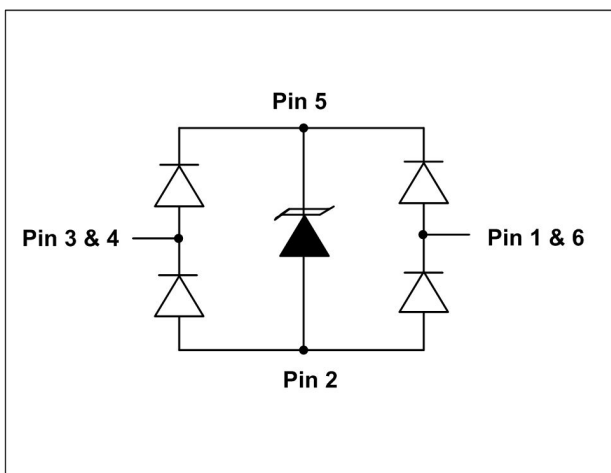
## Mechanical Characteristics

- JEDEC SOT-363 package
- Molding compound flammability rating: UL 94V-0
- Marking : Making Code
- Packaging : Tape and Reel per EIA 481
- RoHS Compliant

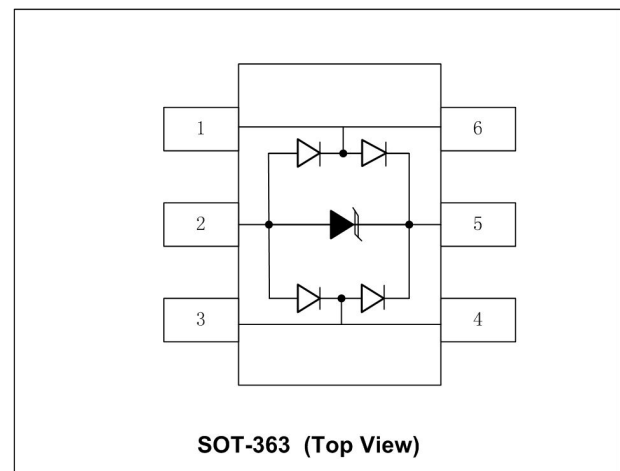
## Applications

- FireWire & USB
- Sensitive Analog Inputs
- Portable Electronics
- LAN/WAN equipment
- Video Line Protection
- Microcontroller Input Protection

## Circuit Diagram



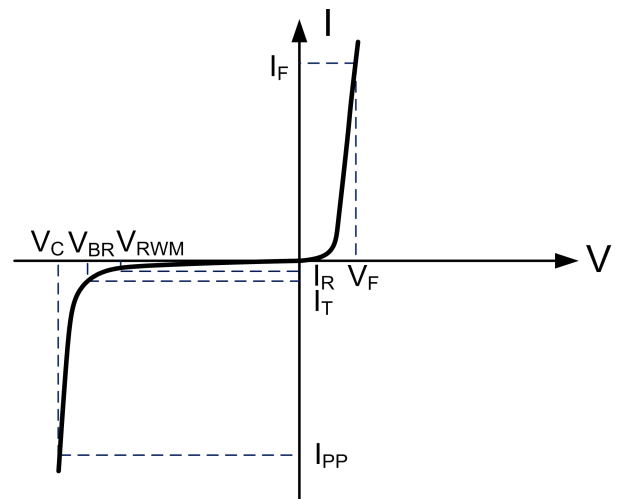
## Schematic & PIN Configuration



Absolute Maximum Rating			
Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p=8/20\mu s$ )	$P_{PP}$	100	Watts
Peak Pulse Current ( $t_p=8/20\mu s$ )	$I_{PP}$	4	A
Lead Soldering Temperature	$T_L$	260(10sec)	$^{\circ}C$
Operating Temperature	$T_J$	-55 to + 125	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55 to +150	$^{\circ}C$

## Electrical Parameters (T=25 $^{\circ}C$ )

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$



## Electrical Characteristics

DW05-2RT3-E						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				5.0	V
Breakdown Voltage	$V_{BR}$	$I_T=1mA$	6.0			V
Reverse Leakage Current	$I_R$	$V_{RWM}=5V, T=25^{\circ}C$			1.0	$\mu A$
Clamping Voltage	$V_C$	$I_{PP}=1A, t_p=8/20\mu s$		10		V
Clamping Voltage	$V_C$	$I_{PP}=4A, t_p=8/20\mu s$		25		V
Junction Capacitance	$C_j$	Between I/O pins and Ground $V_R=0V, f=1MHz$		0.8	1.0	pF
		Between I/O pins $V_R=0V, f=1MHz$		0.4	0.6	pF



## Typical Characteristics

Figure 1: Peak Pulse Power Vs Pulse Time

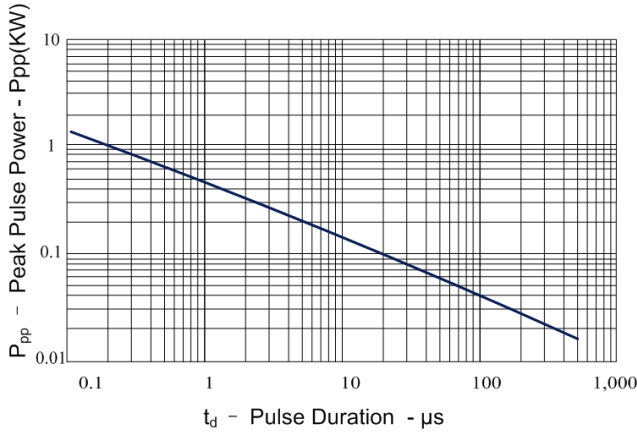


Figure 2: Power Derating Curve

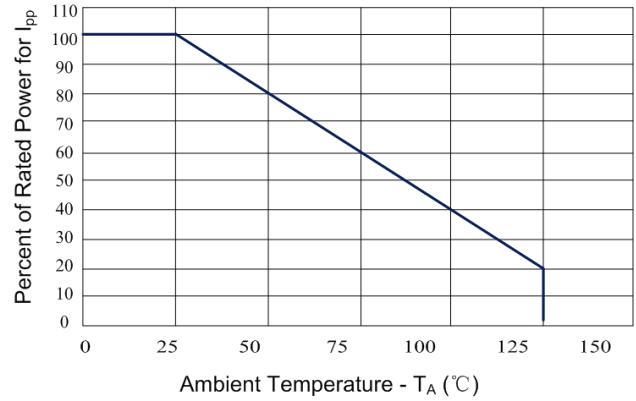


Figure 3: Pulse Waveform

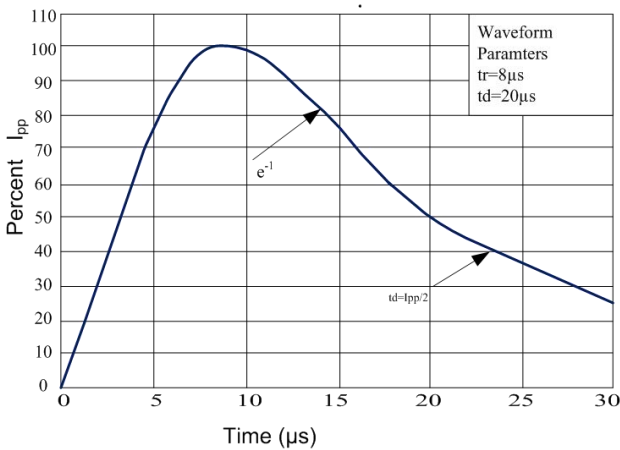


Figure 4: Clamping Voltage vs. Peak Pulse Current

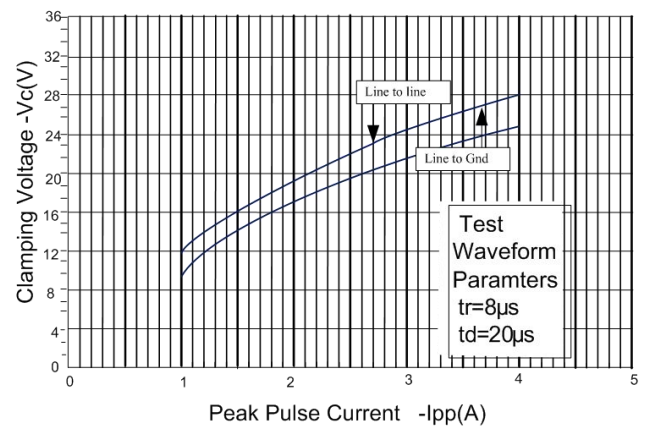


Figure 5: Forward Voltage vs. Forward Current

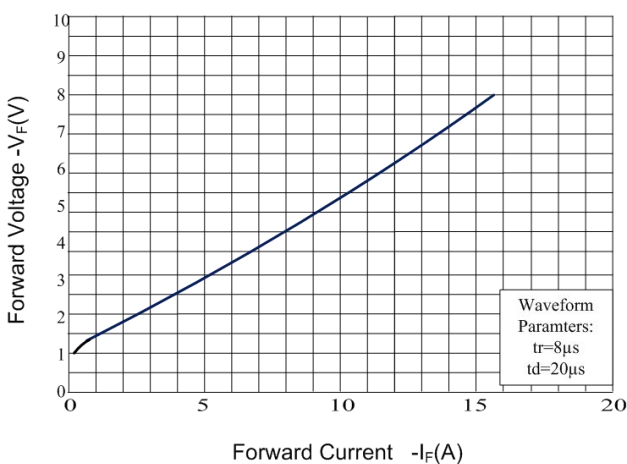
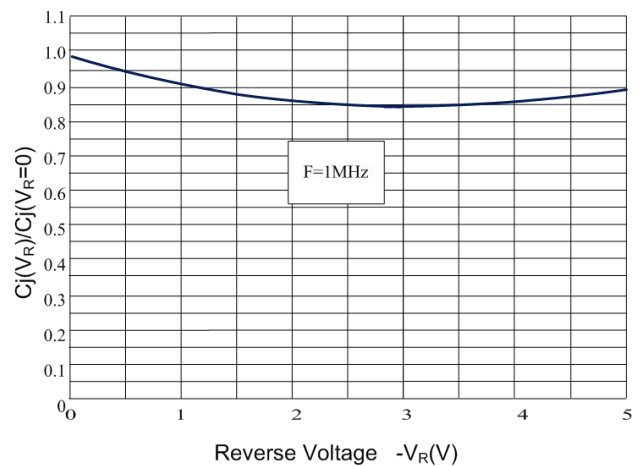


Figure 6: Capacitance vs. Reverse Voltage

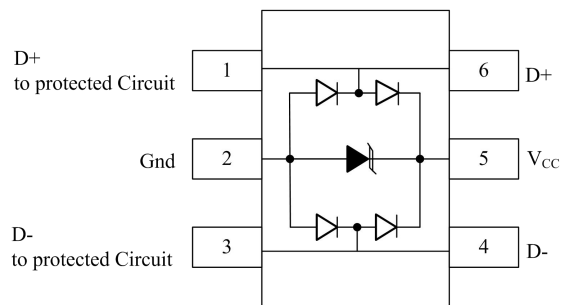


## Application Information

### USB2.0 ESD Protection

The DW05-2RT3-E may also be used to protect both upstream and downstream USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to one USB port (Figure 1). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

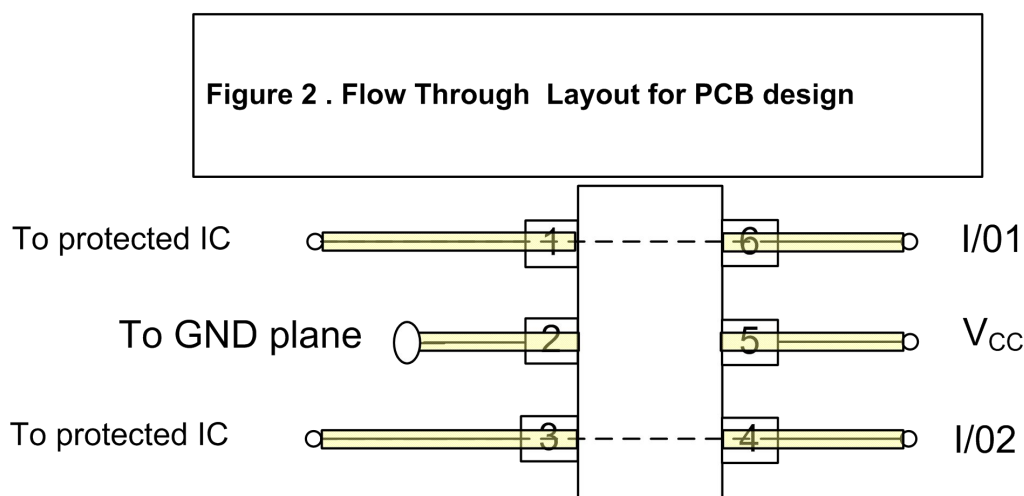
Figure 1. USB Upstream or Downstream Port ESD Protection



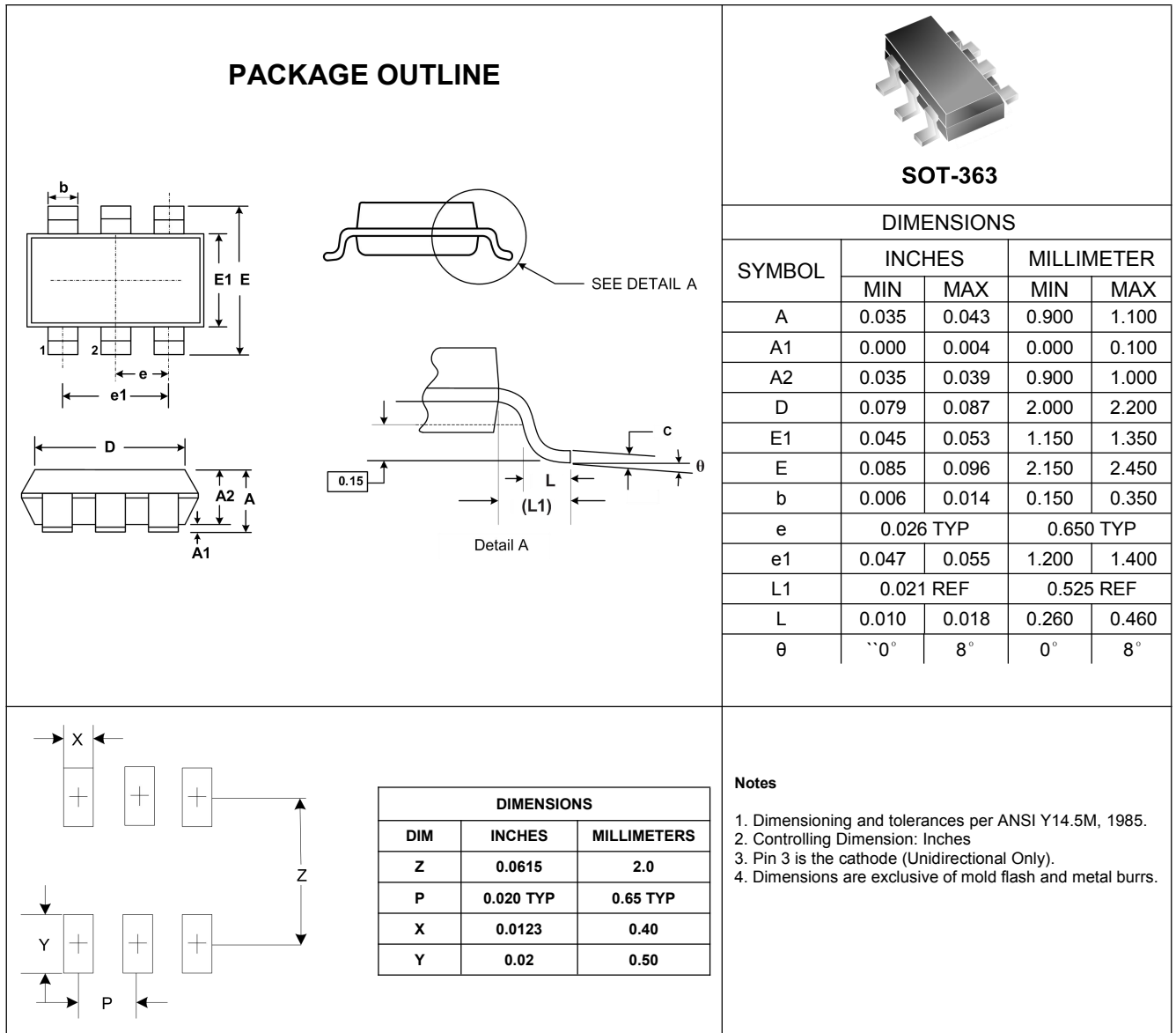
### PCB Layout

Figure 2 shows the proper way to design the PCB board trace in order to use the flow through layout for two line pairs. The solid line represents the PCB trace. Note the PCB traces are used to connect the pin pairs for each I/O (pin 1 to pin 6 and pins 3 to pin 4). For example, I/O 1 enters at pin 6 and exits at pin 1 and the PCB trace connects pins 6 and 1 together. This is also true for I/O 2. The negative reference (Gnd) is connected at pin 2. The positive reference is connected at pin 5..

Figure 2 . Flow Through Layout for PCB design



## Outline Drawing – SOT-363



## Marking Codes

Part Number	DW05-2RT3-E
Marking Code	5R3

## Package Information

Qty: 3k/Reel